MS108: Computer System 1

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Final Project

Due: June. 17th, 2015

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Collaboration Policy

You are allowed to team up with 2 people maximum per group. Both of you will be presenting the project before me, and I will be randomly assigning questions for you to answer. This means each of you should be prepared to answer every aspect of your final project and design.

Project Requirement

1. You will be designing a MIPS compatible microprocessor. You need to support basic MIPS instructions such as add, sub, shift, multiply, branch, loadd/store, etc. All the arithmetic blocks should be designed with Verilog behavior model. There is absolutely NO need to design detailed circuit implementation for the arithmetic blocks.
2. You must design a five stage pipelined microprocessor as described in the lecture. Clearly label all the pipeline registers in your design. All the arithmetic operations take a single cycle to complete. This is a single issue machine.
3. The access to memory takes 200 cycles to complete. This is too long and you need to design a cache to hide the latency. You only need to design level one cache. The cache design choice is up to you. You need to design a cache that can be implemented in hardware.
4. You are required to design a branch predictor. The detailed design choice is up to you. The predictor should at least be able to capture for-loop style code.

Testing Program

The testing program is to add 100 random numbers. The 100 random numbers should be stored in an array in the memory. The processor needs to read out from the memory array one by one the number and use a sum register to accumulate. The final result will be stored back to the memory. You need to write you own MIPS assembly code to achieve the function designed above. In your presentation, I will provide you a text file containing the 100 numbers (in hex format). Your design need to read in the file, copy the data into your main memory and your processor should execute the program to calculate the result.

Evaluation

The scoring will be based on three aspects:

1. Correctness: whether your program can correctly execute the program and calculate the correct answer. I will also check the waveform of your design to confirm.
2. Performance: how fast your processor can execute the program. Depending on your cache and branch predictor design, I will evaluate the design quality.
3. Presentation: this is based on the question-and-answer during the presentation. I will also check your coding style and occasionally, I will ask you to modify your code to achieve some new functionality.
4. Final report: you need to hand-in a high quality final report describing your design solutions.

Tools and Language

You will be using Verilog-HDL to model the processor. Modelsim will be your default simulation platform. You need to learn the basic skills to model logic circuit and write test benches for hardware simulation.

What to submit

1. The complete design source files, including the test benches.
2. The assembly code you used to execute the program.
3. A final report describing your design.